Migration Guide for Micron MT25QL to Infineon S25FL-S Quad SPI Flash

About this document

Scope and purpose

This application note provides guidelines for migration from Micron's MT25QL to Infineon S25FL-S Quad SPI Flash memory products. It describes the similarities and differences in specifications to facilitate this migration.

Intended audience

This is intended for flash memory users who intend to migrate from Micron's MT25QL to Infineon S25FL-S Quad SPI flash.

Table of contents

1 Introduction

This Migration Guide compares the functionalities described in Micron MT25QL and Infineon S25FL-S datasheets. It details the similarities and differences between these two device families to facilitate the migration efforts. No actual tests are performed to verify the migration results. For specific device information, refer to their individual datasheets.

2 Features Comparison

Table 1 Features Comparison

Feature/Parameter	MT25QL	S25FL-S
Densities	128 Mb, 256 Mb, and 512 Mb	128 Mb, 256 Mb, and 512 Mb
Bus Width	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7 V–3.6 V	2.7 V–3.6 V
Normal Read Speed (SIO)	6.75 MB/s (54 MHz)	6.25 MB/s (50 MHz)
Fast Read Speed (SIO)	17 MB/s (133 MHz)	17 MB/s (133 MHz)
Dual Read Speed (DIO)	33 MB/s (133 MHz)	26 MB/s (104 MHz)
Quad Read Speed (QIO)	62 MB/s (133 MHz)	52 MB/s (104 MHz)
Quad Read Speed (QIO - DDR)	90 MB/s (90 MHz)	80 MB/s (80 MHz)
Program Buffer Size	256B	256B or 512B
Erase Sector Size	4 KB / 32 KB/ 64 KB	64 KB or 256 KB
Parameter Sector Size	4 KB	4 KB[1]
Security Region / OTP	64 Bytes	1024 Bytes
Data Protection	Legacy Protection Advanced Security Protection	Legacy Protection Advanced Sector Protection
Suspend / Resume	Erase / Program	Erase / Program
Addressing	3-Byte, 4-Byte	3-Byte, 4-Byte
Hardware Reset	Yes	Yes
Operating Temperature	–40°C to +125°C	–40°C to +125°C
Deep Power Down	Yes	Not supported
XIP Mode	Yes	Yes
ID and SFDP	Read ID and SFDP	Read ID SFDP (FL512S)
Packages	16-pin SOIC (300 mils) 8-Contact WSON (6 × 8 mm) 24-Ball FBGA (6 × 8 mm) 5x5	16-pin SOIC (300 mils) 8-Contact WSON (6 × 8 mm) (FL128S & FL256S) 24-Ball FBGA (6 × 8 mm) 5x5 24-Ball FBGA (6 × 8 mm) 6x4

Note: S25FL-S uses Mode cycle to support the XIP function, but MT25QL uses registers to enter and exit XIP mode.

1 S25FL128S and S25FL256S only

3 Sector Architecture

Micron MT25QL devices have a uniform sector size of 64 KB. They also offer subsector erase size of 4 KB and 32 KB. Infineon S25FL-S family has two options for sector architecture depending on the Ordering Part Number (OPN). One is a hybrid sector size option with 64-KB sectors and 4-KB parameter sectors. Another option is uniform 256-KB sectors. S25FL512S has uniform 256-KB sectors, and no 4-KB parameter sectors. Depending on the application, you can choose the OPN to order to migrate from the Micron device.

The following tables show detailed sector address maps in S25FL-S devices with different configurations.

Table 2 S25FL128S Sector Address Map, Bottom 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	32	SA00	00000000h-00000FFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA31	0001F000h-0001FFFFh	
64	254	SA32	00020000h-0002FFFFh	
		…	…	
		SA285	00FF0000h-00FFFFFFh	

Table 3 S25FL128S Sector Address Map, Top 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	254	SA00	00000000h-0000FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA253	00FD0000h-00FDFFFFh	
4	32	SA254	00FE0000h-00FE0FFFh	
		…	…	
		SA285	00FFF000h-00FFFFFFh	

Table 4 S25FL128S Sector Address Map, Uniform 256-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
256	64	SA00	00000000h-0003FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA63	00FC0000h-00FFFFFFh	

Sector Architecture

Table 5 S25FL256S Sector Address Map, Bottom 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	32	SA00	00000000h-00000FFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA31	0001F000h-0001FFFFh	
64	510	SA32	00020000h-0002FFFFh	
		…	…	
		SA541	01FF0000h-01FFFFFFh	

Table 6 S25FL256S Sector Address Map, Top 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	510	SA00	00000000h-0000FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA509	01FD0000h-01FDFFFFh	
4	32	SA510	01FE0000h-01FE0FFFh	
		…	…	
		SA541	01FFF000h-01FFFFFFh	

Table 7 S25FL256S Sector Address Map, Uniform 256-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
256	128	SA00	00000000h-0003FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA127	01FC0000h-01FFFFFFh	

Table 8 S25FL512S Sector Address Map, Uniform 256-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
256	256	SA00	00000000h-0003FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA255	03FC0000h-03FFFFFFh	

4 Command Set Comparison

Table 9 summarizes the software command set supported in Micron MT25QL and Infineon S25FL-S devices. Subsequent sections discuss pertinent differences between the devices.

Table 9 Command Set Comparison

Function	Command	Description	MT25QL	S25FL-S
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9Eh/9Fh	9Fh
	READ_ID	Read Electronic Manufacturer Signature	–	90h
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	5Ah[2]
	RDQID	Read Quad ID	AFh	–
Reset	RSTEN	Software Reset Enable	66h	–
	RST/RESET	Software Reset	99h	F0h
Deep Power Down	DPD	Deep Power Down	B9h	–
	RES	Release from DPD / Electronic Signature Read	ABh	ABh
Register Access	RDSR	Read Status Register	05h	05h
	RDSR2	Read Status Register 2	–	07h
		Read Flag Status Register	70h	–
	RDCR	Read Configuration Register 1	–	35h
		Read Non-volatile Configuration Register	B5h	–
		Read Volatile Configuration Register	85h	–
		Read Enhanced Volatile Configuration Register	65h	–
		Read General Purpose Read Register	96h	–
	WRR	Write Register	01h	01h
		Write Non-volatile Configuration Register	B1h	–
		Write Volatile Configuration Register	81h	–
		Write Enhanced Volatile Configuration Register	61h	–
	CLSR	Clear Status Register	50h	30h
	ABRD	AutoBoot Register Read	–	14h
	ABWR	AutoBoot Register Write	–	15h
	BRRD	Bank Register Read	–	16h
	BRWR	Bank Register Write	–	17h
	ECCRD	ECC Read	–	18h
4-Byte Mode ≥256 Mb)		Enter 4-Byte Address Mode	B7h	–

2 S25FL512S only

Command Set Comparison

Function	Command	Description	MT25QL	S25FL-S
		Exit 4-Byte Address Mode	E9h	–
Read Flash Array	READ	Read (1-1-1)	03h	03h
	FAST_READ	Fast Read (1-1-1)	0Bh	0Bh
	DOR	Dual Output Read (1-1-2)	3Bh	3Bh
	QOR	Quad Output Read (1-1-4)	6Bh	6Bh
	DIOR	Dual I/O Read (1-2-2)	BBh	BBh
	QIOR	Quad I/O Read (1-4-4)	EBh	EBh
	DDRFR	DDR Fast Read (1-1-1)	0Dh	0Dh
		DDR Dual Output Read (1-1-2)	3Dh	–
		DDR Quad Output Read (1-1-4)	6Dh	–
	DDRDIOR	DDR Dual I/O Read (1-2-2)	BDh	BDh
	DDRQIOR	DDR Quad I/O Read (1-4-4)	EDh	EDh
	QIOWR	Quad I/O Word Read (1-4-4)	E7h	–
	4READ	4-Byte Read (1-1-1)	13h	13h
	4FAST_READ	4-Byte Fast Read (1-1-1)	0Ch	0Ch
	4DOR	4-Byte Dual Output Read (1-1-2)	3Ch	3Ch
	4QOR	4-Byte Quad Output Read (1-1-4)	6Ch	6Ch
	4DIOR	4-Byte Dual I/O Read (1-2-2)	BCh	BCh
	4QIOR	4-Byte Quad I/O Read (1-4-4)	ECh	ECh
	4DDRFR	4-Byte DDR Read (1-1-1)	0Eh	0Eh
	4DDRDIOR	4-Byte DDR Dual I/O Read (1-2-2)	BEh	BEh
	4DDRQIOR	4-Byte DDR Quad I/O Read (1-4-4)	EEh	EEh
Write Operations	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
Program Flash Array	PP	Page Program (1-1-1)	02h	02h
		Dual Input Fast Program (1-1-2)	A2h	–
		Extended Dual Input Fast Program (1-2-2)	D2h	–
	QPP	Quad Input Fast Program (1-1-4)	32h	32h
		Extended Quad Input Fast Program (1-4-4)	38h	38h[3]
	4PP	4-Byte Page Program (1-1-1)	12h	12h
	4QPP	4-Byte Quad Input Fast Program (1-1-4)	34h	34h
		4-Byte Quad Input Extended Fast Program (1-4-4)	3Eh	–
Erase Flash Array	P4E	4-KB SubSector Erase	20h	20h[4]

3 38h in S25FL-S has 1-1-4 format just like the 32h command.

4 20h and 21h work for bottom or top 4-KB parameter sectors in S25FL128S and S25FL256S.

Command Set Comparison

Function	Command	Description	MT25QL	S25FL-S
		32-KB SubSector Erase	52h	–
	SE	Sector Erase	D8h	D8h
	CE	Chip Erase / Bulk Erase	C7h/60h	C7h/60h
	4SE	4-Byte Sector Erase	DCh	DCh
	4P4E	4-Byte 4-KB SubSector Erase	21h	21h3
		4-Byte 32-KB SubSector Erase	5Ch	–
Erase Suspend / Resume	EPS	Erase Suspend	75h	75h
	EPR	Erase Resume	7Ah	7Ah
Program Suspend / Resume	PGSP	Program Suspend	75h	85h
	PGRS	Program Resume	7Ah	8Ah
One-Time Programmable (OTP) Array	OTPR	OTP Read	4Bh	4Bh
	OTPP	OTP Program	42h	42h
Array Protection	ASPRD	ASP Read	–	2Bh
	ASPP	ASP Program	–	2Fh
	PLBWR	PPB Lock Bit Write	–	A3h
	PLBRD	PPB Lock Bit Read	–	A6h
	DYBRD	DYB Read	–	E0h
	DYBWR	DYB Write	–	E1h
	PPBRD	PPB Read	–	E2h
	PPBWR	PPB Write	–	E3h
	PPBE	PPB Erase	–	E7h
	PASSRD	Password Read	–	E8h
	PASSP	Password Program	–	E3h
	PASSU	Password Unlock	–	E9h
		Read Sector Protection	2Dh	–
		Program Sector Protection	2Ch	–
		Read Volatile Lock Bits	E8h	–
		Write Volatile Lock Bits	E5h	–
		Read Non-volatile Lock Bits	E2h	–
		Write Non-volatile Lock Bits	E3h	–
		Erase Non-volatile Lock Bits	E4h	–
		Read Global Freeze Bit	A7h	–
		Write Global Freeze Bit	A6h	–
		Read Password	27h	–
		Write Password	28h	–
		Unlock Password	29h	–
Data Learning Pattern	DLPRD	Data Learning Pattern Read	–	41h
	PNVDLR	Program NV Data Learning Pattern	–	43h
		Interface Activation	9Bh	–

Function	Command	Description	MT25QL	S25FL-S
Advanced Function Interface		Cyclic Redundancy Check	9Bh/27h	–

4.1 Identification Commands

MT25QL devices can use either 9Eh or 9Fh to read the device ID. S25FL-S supports the 9Fh command only.

For Serial Flash Discoverable Parameters (SFDP) data, only S25FL512S supports this function. S25FL128S or S25FL256S does not support it.

There are no Multi IO reads for ID commands in S25FL-S.

4.2 Reset Command

MT25QL devices use the sequence 66h and 99h to perform a software reset. S25FL-S can be reset by just a one-byte command, F0h.

4.3 Deep Power Down

There is no Deep Power Down function in S25FL-S. However, the ABh command will return the Electronic Signature from the device in S25FL-S.

4.4 Status and Configuration Registers

Status Registers and Configuration Registers are defined quite differently in MT25QL and S25FL-S devices. The basic Status Register has some similar bits but all other registers are different. You must look at the bits that are currently being used with MT25QL and find the corresponding registers in S25FL-S.

Only the basic read, write, and clear Status Register commands are common in these two devices. Other register access commands in MT25QL are not supported in S25FL-S.

4.5 4-Byte Address Mode

In devices with higher capacities than 256 Mb, 4-Byte addressing scheme is needed. Both MT25QL and S25FL-S provide a different set of commands that support 4-Byte addressing. This is the most straight forward way to access the full range of the device.

If you prefer to keep the old command values but want to use 4-Byte addressing, MT25QL supports a 4-Byte Address Mode that can be entered or exited with a command.

Table 10 Micron MT25QL 4-Byte Address Mode Operations

Operation Name	Description/Conditions
ENTER 4-BYTE ADDRESS MODE (B7h)	The effect of the command is immediate. The default address mode is three bytes, and the device returns to the default upon exiting the 4-byte address mode.
EXIT 4-BYTE ADDRESS MODE (E9h)	

You can use Bit 7 of the Bank Register in S25FL-S devices to support the 4-Byte Addressing Mode. Setting this bit to ‘1’ allows you to continue to use old 3-Byte Addressing commands but with 4-Byte Addressing.

Table 11 Infineon S25FL-S Bank Register

Bits	Field Name	Function	Type	Default State	Description
7	EXTADD	Extended Address Enable	Volatile	0b	1 = 4-byte (32-bits) addressing required from command. 0 = 3-byte (24-bits) addressing from command + Bank Address
6 to 2	RFU	Reserved	Volatile	00000b	Reserved for Future Use
1	BA25	Bank Address	Volatile	0	A25 for 512 Mb device
0	BA24	Bank Address	Volatile	0	A24 for 512 Mb device

During the migration, you must look at how the existing software implemented the 4-Byte Addressing scheme and make changes according to the S25FL-S specifications.

4.6 Read Access Commands

Most read commands are compatible in both MT25QL and S25FL-S devices. Both of them support Normal Read (1-1-1), Fast Read (1-1-1), Dual Output Read (1-1-2), Quad Output Read (1-1-4), Dual I/O Read (1-2-2), Quad I/O Read (1-4-4), DDR Read (1-1-1), DDR Dual I/O Read (1-2-2), and DDR Quad I/O Read (1-4-4). However, specifically, DDR Dual Output Read (1-1-2) and DDR Quad Output Read (1-1-4) are not supported in S25FL-S.

Some read commands require a read latency to allow time to access the flash memory array. The read latency cycles are traditionally called dummy cycles. The dummy cycles are defined in Non-volatile Configuration Register in MT25QL, while they are defined in Configuration Register 1 in S25FL-S. Look up the definitions of how the read latency is defined in each datasheet to find the appropriate settings.

Table 12 shows the Latency Code definitions in CR1.

Table 12 Infineon S25FL-S CR1 LC Bits

Bits	Field Name	Function	Type	Default State	Description
7	LC1	Latency Code	Non-Volatile	0	Selects number of initial read latency cycles See Latency Code Tables
6	LC0			0	

The 2-bit LC field selects the number of mode and dummy cycles between the end of address and the start of the read data output. When ordering S25FL-S devices, there are two ordering options regarding to the LC bit definitions, High Performance LC (HPLC) and Enhanced High Performance LC (EHPLC). In each mode, the values of LC bits correspond to different sets of mode and dummy cycles settings.

Refer to **Table 13** through **Table 16** for each LC bit settings.

Table 13 Latency Codes for SDR HPLC

Freq. (MHz)	LC	Read (03h, 13h)		Fast Read (0Bh, 0Ch)		Read Dual Out (3Bh, 3Ch)		Read Quad Out (6Bh, 6Ch)		Dual I/O Read (BBh, BCh)		Quad I/O Read (EBh, ECh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	0	0	0	0	0	0	0	0	0	4	2	1
≤ 80	00	-	-	0	8	0	8	0	8	0	4	2	4
≤ 90	01	-	-	0	8	0	8	0	8	0	5	2	4
≤104	10	-	-	0	8	0	8	0	8	0	6	2	5
≤133	10	-	-	0	8	-	-	-	-	-	-	-	-

Table 14 Latency Codes for DDR HPLC

Freq. (MHz)	LC	DDR Fast Read (0Dh, 0Eh)		DDR Dual I/O Read (BDh, BEh)		Read DDR Quad I/O (EDh, EEh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	0	4	0	4	1	3
≤ 66	00	0	5	0	6	1	6
≤ 66	01	0	6	0	7	1	7
≤ 66	10	0	7	0	8	1	8

Table 15 Latency Codes for SDR EHPLC

Freq. (MHz)	LC	Read (03h, 13h)		Fast Read (0Bh, 0Ch)		Read Dual Out (3Bh, 3Ch)		Read Quad Out (6Bh, 6Ch)		Dual I/O Read (BBh, BCh)		Quad I/O Read (EBh, ECh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	0	0	0	0	0	0	0	0	4	0	2	1
≤ 80	00	-	-	0	8	0	8	0	8	4	0	2	4
≤ 90	01	-	-	0	8	0	8	0	8	4	1	2	4
≤104	10	-	-	0	8	0	8	0	8	4	2	2	5
≤133	10	-	-	0	8	-	-	-	-	-	-	-	-

Table 16 Latency Codes for DDR EHPLC

Freq. (MHz)	LC	DDR Fast Read (0Dh, 0Eh)		DDR Dual I/O Read (BDh, BEh)		Read DDR Quad I/O (EDh, EEh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	4	1	2	2	1	3
≤ 66	00	4	2	2	4	1	6
≤ 66	01	4	4	2	5	1	7
≤ 66	10	4	5	2	6	1	8
≤ 80	00	4	2	2	4	1	6
≤ 80	01	4	4	2	5	1	7
≤ 80	10	4	5	2	6	1	8

4.7 Program Commands

Both MT25QL and S25FL-S support normal Page Programming (1-1-1), and Quad Programming (1-1-4) commands. Dual Input Program (1-1-2), Extended Dual Input Program (1-2-2), and Extended Quad Input Program (1-4-4) are not supported in S25FL-S.

4.8 Dual I/O and Quad I/O Modes

In MT25QL devices, you can enter Dual I/O mode (2-2-2) or Quad I/O mode (4-4-4) for all commands by setting the corresponding bits in the Enhanced Volatile Configuration Register. These two modes are not supported in S25FL-S devices.

4.9 Erase Commands

Both MT25QL and S25FL-S have 64-KB physical sectors. The Sector Erase command is the same. MT25QL provides subsector erase commands for 4-KB and 32-KB subsectors. S25FL-S does not provide the 32 KB erase command. In S25FL128S and S25FL256S, there is an option to have thirty-two 4-KB sectors on the bottom or on the top of the device. In such case, 4 KB Erase command is supported.

S25FL-S devices also provide uniform 256-KB sector option, which does not exist in MT25QL devices.

4.10 Suspend and Resume

Both MT25QL and S25FL-S support Erase and Program Suspend and Resume commands. In MT25QL, there is one suspend command for both Erase and Program, same for the resume command. However, in S25FL-S, the Erase Suspend and Resume commands are the same as in MT25QL; however, the Program Suspend and Resume commands have different values.

4.11 OTP Area

MT25QL has a dedicated 64-Byte OTP area outside of the main memory array. S25FL-S has 1024-Byte OTP area. To read or program this area, the commands are the same in these two devices.

To protect the OTP area, the methods in these two devices are different. Refer to individual datasheets for the OTP protection methods.

4.12 Array Protection

Both MT25QL and S25FL-S provide legacy protection through BP bits. Furthermore, they both provide individual sector volatile and non-volatile protections through registers. However, the ways of accessing these registers in MT25QL are quite different from S25FL-S. You must modify the software to support a totally new scheme of Advanced Sector Protection as described in the S25FL-S datasheet.

5 Hardware Comparison

5.1 Package Compatibility

Table 17 shows the supported packages in MT25QL and S25FL-S families. For densities 128 Mb or 256 Mb, SOIC-8 and WSON 5×6 mm packages are not supported in S25FL-S family.

Table 17 Package Compatibility

Package Name	MT25QL	S25FL-S
8-pin SOIC (208 mil)	✓[5]	
16-pin SOIC (300 mil)	✓	✓
8-Contact WSON (5 × 6 mm)	✓[6]	
8-Contact WSON (6 × 8 mm)	✓	✓
5 x 5 24-ball FBGA (6 × 8 mm)	✓	✓
4 x 6 24-ball FBGA (6 × 8 mm)	✓	✓

5.2 Signal Compatibility

Table 18 shows the Signal Pins comparison in MT25QL and S25FL-S families. All signals are compatible in both device families.

Table 18 Signal Compatibility

MT25QL Signal	S25FL-S Signal	Description
S#	CS#	Chip Select
C	SCK	Serial Clock
DQ[3:0]	IO[3:0]	Data input and output
W#	WP#	Write Protect (IO2)
HOLD#	HOLD#	Hold (IO3)
RESET#	RESET#	Dedicated reset pin
Vcc	Vcc	Power Supply
Vss	Vss	Ground

5.3 DC Characteristics

Table 19 shows a comparison of basic DC parameters for MT25QL and S25FL-S. For the complete parameters details specified, refer to the datasheets.

Table 19 DC Parameters Comparison

Symbol	Operating Parameter	MT25QL			S25FL-S			Unit
		Min	Typical	Max	Min	Typical	Max	
V_{CC}	V_{CC} (Supply voltage)	2.7	–	3.6	2.7	–	3.6	V
V_{IL}	Input Low Voltage	–0.5	–	0.3 x V_{CC}	–0.3	–	0.3 x V_{IO}	V

5 128 Mb only

6 128 Mb and 256 Mb only

Symbol	Operating Parameter	MT25QL			S25FL-S			Unit
		Min	Typical	Max	Min	Typical	Max	
V_{IH}	Input High Voltage	0.7 x V_{CC}	–	V_{CC} + 0.4	0.7 x V_{CC}	–	V_{IO} +0.4	V
V_{OL}	Output Low Voltage	–	–	0.4		–	0.15 x V_{IO}	V
V_{OH}	Output High Voltage	V_{CC} – 0.2	–		0.85 x V_{IO}	–		V
I_{LI}	Input Leakage Current	–	–	±2	–	–	±2	µA
I_{LO}	Output Leakage Current	–	–	±2	–	–	±2	µA
I_{CC1}	Active Power Supply Current (READ) – Serial SDR@133 MHz	–	–	16	–	–	33	mA
	Active Power Supply Current (READ) – Quad DDR@80 MHz	–	–	28	–	–	90	mA
I_{CC2}	Active Power Supply Current (Page Program)	–	–	35	–	–	100	mA
I_{CC3}	Active Power Supply Current (WRR or WRAR)	–	–	35	–	–	100	mA
I_{CC4}	Active Power Supply Current (SE)	–	–	35	–	–	100	mA
I_{SB}	Standby Current (Industrial)	–	30	75	–	70	100	µA
	Standby Current (Industrial Plus)	–	30	200	–	70	300	µA
I_{DPD}	Deep Power Down Current	–	5	50	–	–	–	µA

5.4 AC Characteristics

Table 20 shows a comparison of basic AC parameters for MT25QL and S25FL-S. For the complete parameters details specified, refer to the datasheets.

Table 20 AC Characteristics Comparison

Symbol	Parameter	MT25QL		S25FL-S		Unit
		Min	Max	Min	Max	
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	–	54	–	50	MHz
$F_{SCK, C}$	SCK Clock Frequency for dual and quad commands	–	133	–	133	MHz
t_{WH}, t_{CH}	Clock HIGH Time	3.375	–	45%/F_{SCK}	–	ns

Symbol	Parameter	MT25QL		S25FL-S		Unit
		Min	Max	Min	Max	
t_{WL}, t_{CL}	Clock LOW Time	5	–	45%/F_{SCK}	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	0.1	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	0.1	–	V/ns
t_{CS}	CS# HIGH Time (Any Read Instructions)	20	–	10	–	ns
	CS# HIGH Time (All other Non-Read instructions)	50	–	50	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3.375	–	3	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3.375	–	3	3000[7]	ns
t_{SU}	Data in Setup Time	1.5	–	1.5	–	ns
t_{HD}	Data in Hold Time	1.5	–	2	–	ns
t_V	Clock LOW to Output Valid	–	6	–	8	ns
t_{HO}	Output Hold Time	1.5	–	2	–	ns
t_{DIS}	Output Disable Time	–	7	–	8	ns
t_{WPS}	WP# Setup Time	20	–	20	–	ns
t_{WPH}	WP# Hold Time	100	–	100	–	µs

5.5 Embedded Algorithms Performance

Table 21 shows a comparison of the program and erase performance for MT25QL and S25FL-S. For details of Program and Erase operations, refer to the datasheets.

Table 21 Program and Erase Performance Comparison

Symbol	Parameter		MT25QL		S25FL-S		Unit
			Typical	Max	Typical	Max	
t_W	Non-volatile Register Write Time		200	1000	140[8] 500[9]	5601 20002	ms
t_{PP}	Page Programming (256 Bytes)		120	2800	250	750	µs
t_{BE}	Block Erase Time (64-KB sectors)		150	1000	1301	6501	ms
t_{CE}	Chip Erase Time	128 Mb	38	114	33	165	sec
		256 Mb	77	231	66	330	
		512 Mb	153	460	103	460	

7 Maximum value only applies during Program/Erase Suspend/Resume commands
8 128 Mb and 256 Mb
9 512 Mb

6 Conclusion

The Infineon S25FL-S device is pin-to-pin compatible with Micron MT25QL. To migrate to S25FL-S, you can keep most basic SPI commands but software modification efforts are needed to accommodate the sector architecture, register sets, and data protection methods offered by the MT25QL family.

References

[1] S25FL128S/ S25FL256S

- **001-98283: S25FL128S/S25FL256S 128 Mbit (16 Mbyte)/256 Mbit (32 Mbyte) 3.0V SPI Flash Memory**

[2] S25FL512S:

- **001-98284: S25FL512S 512 Mbit (64 Mbyte), 3.0 V SPI Flash Memory**

Revision history

Document version	Date of release	Description of changes
**	2018-03-26	New application note.
*A	2021-04-30	Updated to Infineon template

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